SERIAL PRESENCE DETECT

HYMP125F72CP8N3-C4/Y5

Byte Number	Function described	Function supported		Hex Value	
		C4	Y5	C4	Y5
0	Number of Serial PD Bytes written/SPD Device Size/CRC Coverage	176 /256 /116 Bytes	176 /256 /116 Bytes	92	92
1	SPD Revision	1.1	1.1	11	11
2	Key Byte / DRAM Device Type	DDR2 SDRAM FB-DIMM	DDR2 SDRAM FB-DIMM	09	09
3	Voltage Levels of this Assembly	1.5V / 1.8V	1.5V / 1.8V	12	12
4	SDRAM Addressing(Row /Column / Bank)	14 / 10 / 8	14 / 10 / 8	45	45
5	Module Phisical Attributes	30.35mm/≤9.0 mm	30.35mm/≤9.0 mm	24	24
6	Module Type / Thickness	FB-DIMM	FB-DIMM	07	07
7	Module Organization	2R/ x8	2R/ x8	11	11
8	Fine Timebase Dividened	10 ps / 1	10 ps / 1	A1	A1
9	Medium Timebase Dividened and Divisor	1ns	1ns	01	01
10	Medium Timebase Divisor	4	4	04	04
11	SDRAM Minimum Cycle Time(tCKmin)	3.75ns	3ns	0F	0C
12	SDRAM Maximum Cycle Time(tCKmax)	8ns	8ns	20	20
13	SDRAM CAS Latency Supported	3,4	4,5	23	24
14	SDRAM Minimum CAS Latency Time(tAA)	DDR2 533 4-4-4	DDR2 667 5-5-5	3C	3C
15	SDRAM Write Recovery Times Supported	2,3,4	2,3,4,5	32	42
16	SDRAM Write Recovery Time(tWR)	15ns	15ns	3C	3C
17	SDRAM Write Latency Supported	2,3,4,5	2,3,4,5	42	42
18	SDRAM Additive Latency Supported	0,1,2,3	0,1,2,3	40	40
19	SDRAM Minimum RAS to CAS Delay (tRCD)	15ns	15ns	3C	3C
20	SDRAM Minimun Row Active to Row Active Delay (tRRD)	7.5ns	7.5ns	1E	1E
21	SDRAM Minimum Row Precharge Time (tRP)	15ns	15ns	3C	3C
22	SDRAM Upper Nibbles for tRAS and tRC	Undefined	Undefined	00	00
23	SDRAM Minimum Active to Precharge Time (tRAS)	45ns	45ns	B4	B4
24	SDRAM Minimum Active to Active / Auto - Refresh Time (tRC)	60ns	60ns	F0	F0
25	SDRAM Min Auto-Refresh to Active / Auto- Refresh Command period (tR	127.5ns	127.5ns	FE	FE
26	SDRAM Min Auto-Refresh to Active / Auto- Refresh Command period (tR	127.5ns	127.5ns	01	01
27	SDRAM Internal Write to Read Command Delay (tWTR)	7.5ns	7.5ns	1E	1E
28	SDRAM Internal Read to Precharge Command Delay (tRTP)	7.5ns	7.5ns	1E	1E
29	SDRAM Burst Lengths Supported	4,8	4,8	03	03
30	SDRAM Termination Supported	50/ 75/ 150Ω	50/ 75/ 150Ω	07	07
31	SDRAM Drivers Supported	Weak driver	Weak driver	01	01
32	SDRAM Average Refresh Interval(tREFI)/Double Refresh mode bit/ High Temperature self-refresh rate support indication	7.8us/ Double Ref./High temp. self ref.	7.8us/ Double Ref./High temp. self ref.	C2	C2
33	DRAM Tcase max / DT4R4W mode bit	95℃/ 0℃	95℃/ 0℃	50	50
34	Thermal resistance of DRAM Package from Top(Case) to Ambient.	69.5℃/W	69.5℃/W	8B	8B
35	DRAM Tcase Rise in IDD0 condtion/Mode Bits(DT0)	5.7℃	6.3℃	4C	54
36	DRAM Tcase Rise in IDD2Q condition(DT2Q)	3.6℃	4℃	24	28
37	DRAM Tcase Rise in IDD2P condition(DT2P)	1.32℃	1.32℃	58	58
38	DRAM Tcase Rise in IDD3N condition(DT3N)	6℃	6.6℃	28	2C
39	DRAM Tcase Rise in IDD4RW condition/Mode Bit(DT4R)	16.4℃	20℃	52	64
40	DRAM Tcase Rise in IDD5B condtion(DT5B)	22℃	23℃	2C	2E
41	DRAM Tcase Rise in IDD7 condtion(DT7)	23℃	24℃	2E	30
42~78	Reserved	Undefined	Undefined	00	00
79	FB-DIMM ODT values			22	22
80	Reserved	Undefined	Undefined	00	00
81	FBD Channel Protocols Supported	ECC	ECC	02	02
82	FBD Channel Protocols Supported	Undefined	Undefined	00	00
83	Back-to-Back Access Turnaround. Time			10	10
84	AMB Read Access Delay for AMB.LINKPARNXT[1:0]=11			56	56
85	AMB Read Access Delay for AMB.LINKPARNXT[1:0]=10			40	40
86	AMB Read Access Delay for AMB.LINKPARNXT[1:0]=01			36	36
87	Thermal Resistance of AMB Package(Psi T-A DRAM)			30	30
88	AMB DT idle_0			52	60
89	AMB DT idle_1			66	7A
90	AMB DT idle_2			60	6E
91	AMB DT Active_1			84	A1
92	AMB DT Active_2			6A	7F
93	AMB DT L0s	Undefined	Undefined	00	00
94~97	Reserved	Undefined	Undefined	00	00
98	AMB Tjmax	Undefined	Undefined	00	00
99	Airflow impedance and category bits	00/ Single Die/FDHS	00/ Single Die/FDHS	0A	0A
100	Reserved	Undefined	Undefined	00	00

101	AMB Personality Bytes:Pre-initialization			80	80
102	AMB Personality Bytes:Pre-initialization			20	20
103	AMB Personality Bytes:Pre-initialization	Undefined	Undefined	00	00
104	AMB Personality Bytes:Pre-initialization			44	44
105	AMB Personality Bytes:Pre-initialization	Undefined	Undefined	04	04
106	AMB Personality Bytes:Pre-initialization	Undefined	Undefined	80	80
107	AMB Personality Bytes:Post-initialization			48	48
108	AMB Personality Bytes:Post-initialization			53	53
109	AMB Personality Bytes:Post-initialization			B3	B3
110	AMB Personality Bytes:Post-initialization	Undefined	Undefined	41	41
111	AMB Personality Bytes:Post-initialization			65	65
112	AMB Personality Bytes:Post-initialization			4C	4C
113	AMB Personality Bytes:Post-initialization	Undefined	Undefined	00	00
114	AMB Personality Bytes:Post-initialization			10	10
115	AMB Manufacturer's JEDEC ID Code			80	80
116	AMB Manufacturer's JEDEC ID Code	Intel	Intel	89	89
117	Module ID: Module Manufacturer JEDEC ID Code			80	80
118	Module ID: Module Manufacturer JEDEC ID Code	Hynix	Hynix	AD	AD
119	Module Manufacturing location	Hynix(Ichon)	Hynix(Ichon)	01	01
120	Module Manufacturing Data (Year)	Year	Year	Variable	Variable
121	Module Manufacturing Data (Week)	WW	WW	Variable	Variable
122-125	Module Serial Number(Main Lot Number)	Undefined	Undefined	00	00
126	Cyclical Redundancy Code	CRC cover 0~116 byte	CRC cover 0~116 byte	60	9C
127	Cyclical Redundancy Code	CRC cover 0~116 byte	CRC cover 0~116 byte	7B	61
128	Manufacture part number (Hynix Memory Module)	H	H	48	48
129	Manufacture part number (Hynix Memory Module)	Y	Y	59	59
130	Manufacture part number (Hynix Memory Module)	M	M	4D	4D
131	Component group (DDR2 SDRAM)	P	P	50	50
132	Component group(DDR2 SDRAM)	1	1	31	31
133	Manufacture part number (Module depth)	2	2	32	32
134	Manufacture part number (Module depth)	5	5	35	35
135	Manufacture part number (Module type)	F	F	46	46
136	Manufacture part number (Data width)	7	7	37	37
137	Manufacture part number (Data width)	2	2	32	32
138	Manufacture part number (Die Generation)	C	C	43	43
139	Manufacture part number (Package Materials)	P	P	50	50
140	Manufacture part number (Component configuration)	8	8	38	38
141	Manufacture part number (AMB Manufacturer)	N	N	4E	4E
142	Manufacture part number (AMB Revision)	3	3	33	33
143	Manufacture part number (Hyphen)	-	-	2D	2D
144	Manufacture part number (Minimum cycle time)	C	Y	43	59
145	Manufacture part number (Minimum cycle time)	4	5	34	35
146	Manufacture revision Code (for Componuent)	Module revision code	Module revision code	00	00
147	Manufacture revision Code (for PCB)	~~Module revision code	~~Module revision code	00	00
148	DRAM Manufacturer JEDEC ID Code	Hynix	Hynix	80	80
149	Manufacturer JEDEC ID Code			AD	AD
150	Manufacturer specific data (may be used in future)	Intel AMB inform rev0.8	Intel AMB inform rev0.8	01	01
151	Manufacturer specific data (may be used in future)			09	09
152~175	Manufacturer specific data (may be used in future)	Undefined	Undefined	00	00
176~255	Open for customer use	Undefined	Undefined	00	00